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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Blakely, Sokoloff, Taylor & Zafman
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER

CERULLO, JEREMY S

ART UNIT	PAPER NUMBER
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2112

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/608,708

Applicant(s)

HAMMARLUND ET AL.

Examiner

Jeremy S. Cerullo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending in this office action.

Claim Objections

2. Claim 5 is objected to because of the following informalities: in the second line of Claim 5, "next a queue" should apparently be "next in a queue". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7-8, 16-17, and 21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Claim 7 recites the limitation "the relinquished resources" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim. There is no previous mention of relinquished resources in Claim 7, 4, or 1.

6. Claim 8 recites the limitation "the relinquishing" in the first line of the claim.

There is insufficient antecedent basis for this limitation in the claim. There is no previous mention of relinquishing in Claim 8, 7, 4, or 1.

7. Claim 16 recites the limitation "the relinquished resources" in the last two lines of the claim. There is insufficient antecedent basis for this limitation in the claim. There is no previous mention of relinquished resources in Claim 16 or 13.

8. Claim 17 recites the limitation "the relinquishing" in the first line of the claim. There is insufficient antecedent basis for this limitation in the claim. There is no previous mention of relinquishing in Claim 17, 16, or 13.

9. Claim 21 recites the limitation "the relinquished resources" in the last two lines of the claim. There is insufficient antecedent basis for this limitation in the claim. There is no previous mention of relinquished resources in Claim 21 or 18.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 4, 22, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,274,809 ("Iwasaki" et al.).

12. As for Claim 1, in Column 2, Lines 15-28, Iwasaki discloses method in which a processor is put to sleep when it fails to lock a resource, which is equivalent to a processor attempting and failing to acquire a contended lock. Iwasaki also discloses that the processor is awakened when the resource is released.

13. As for Claim 4, Iwasaki also discloses in Column 2, Lines 15-28, that the processor is awakened contended locked resource becomes available and that the awakened processor acquires the resource.

14. As for Claim 22, in Column 2, Lines 15-28, Iwasaki discloses method in which a processor is put to sleep when it fails to lock a resource, which is equivalent to a processor attempting and failing to acquire a contended lock. Iwasaki also discloses that the processor is awakened when the resource is released. Iwasaki also discloses a machine-readable medium, memory, (Column 1, Lines 39-47) and it is inherent the actions taken by the processor are in the form of instructions stored in some type of machine-readable medium accessible by the processor.

15. As for Claim 25, Iwasaki also discloses in Column 2, Lines 15-28, that the processor is awakened contended locked resource becomes available and that the awakened processor acquires the resource.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 2-3 and 23-24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki in view of U.S. Patent No. 6,493,741 ("Emer" et al.).

19. As for Claims 2-3, Iwasaki teaches the limitations inherited from Claim 1, but he does not teach the use of MONITOR and MWAIT instructions. However, Emer teaches the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT. It would have been obvious to one of ordinary skill in the art at the time of the

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invention to have used the instructions as taught by Emer in the method of Iwasaki in order put the processor to sleep while it waits for another processor to release the resource, preventing wasting cycles repeating its request.

20. As for Claims 23-24, Iwasaki teaches the limitations inherited from Claim 1, but he does not teach the use of MONITOR and MWAIT instructions. However, Emer teaches the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the instructions as taught by Emer in the method of Iwasaki in order put the processor to sleep while it waits for another processor to release the resource, preventing wasting cycles repeating its request.

21. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki in view of U.S. Patent Application Publication No. 2003/0236816 (Venkatasubramanian, "Ven"). Iwasaki teaches the limitations inherited from Claim 1 (See rejection above), but he does not explicitly teach that the processor is in a queue awaiting the release of the locked resource. However, in Column 2, Lines 25-28. Iwasaki does teach that the processor may have to wait for another task to be completed after the one that currently has locked the resource. While he does not explicitly teach the use of a queue, Ven does teach the use of a sleep queue for threads waiting for a lock. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a

queue as taught by Ven in the method of Iwasaki in order to allow processors access to the resource in the order they requested it, preventing starvation of the sleeping processor.

22. Claims 6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki in view of U.S. Patent No. 6,035,374 ("Panwar" et al.).

23. As for Claim 6, Iwasaki teaches all of the limitations inherited from Claim 1, but he does not teach that putting a processor to sleep comprises the processor relinquishing all of its resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Iwasaki release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

24. As for Claim 26, Iwasaki teaches all of the limitations inherited from Claim 22, but he does not teach that putting a processor to sleep comprises the processor relinquishing all of its resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Iwasaki release its resources as taught by Panwar in order to prevent itself from interfering with the

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execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

25. Claims 9-12 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki and Ven as applied to Claims 5 above, and further in view of Emer as applied to Claims 2-3 and 23-24 above.

26. As for Claims 9-12, Iwasaki and Ven teach a queue of processors awaiting the release of a monitored, locked resource, such that the next processor on the queue acquires the lock upon its release (See rejection of Claim 5 above). They do not teach the use of MONITOR and MWAIT instructions to achieve these actions. However, Emer teaches the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the instructions as taught by Emer in the method of Iwasaki in order put the processor to sleep while it waits for another processor to release the resource, preventing wasting cycles repeating its request.

27. As for Claims 27-30, Iwasaki and Ven teach a queue of processors awaiting the release of a monitored, locked resource, such that the next processor on the queue acquires the lock upon its release (See rejection of Claim 5 above). Iwasaki also teaches a machine-readable medium, memory, (Column 1, Lines 39-47) and it is inherent the actions taken by the processor are in the form of instructions stored in

some type of machine-readable medium accessible by the processor. They do not teach the use of MONITOR and MWAIT instructions to achieve these actions.

However, Emer teaches the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the instructions as taught by Emer in the method of Iwasaki in order put the processor to sleep while it waits for another processor to release the resource, preventing wasting cycles repeating its request.

28. Claims 13-14 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki as applied to claim 1 above, and further in view of Emer as applied to Claims 2-3 and 23-24 above.

29. As for Claims 13-14, Iwasaki teaches a processor awaiting the release of a monitored, locked resource (Column 2, Lines 15-27). He does not teach the use of MONITOR and MWAIT instructions to achieve these actions. However, Emer teaches the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the instructions as taught by Emer in the method of Iwasaki in

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order put the processor to sleep while it waits for another processor to release the resource, preventing wasting cycles repeating its request.

30. As for Claims 18-19, Iwasaki teaches a system with a processor awaiting the release of a monitored, locked resource (Column 2, Lines 15-27). He also teaches that a memory (storage medium) is provided for storing data of the resources (Column 1, Lines 39-47). He does not teach the use of MONITOR and MWAIT instructions to achieve these actions. However, Emer teaches the use of pair of instructions (LDx_ARM and QUIESCE) in order to halt a processor (put it to sleep) while it waits for an event to occur (Column 5, Lines 28-40). LDx_ARM and QUIESCE are functionally equivalent to the claimed instructions, MONITOR and MWAIT. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the instructions as taught by Emer in the method of Iwasaki in order put the processor to sleep while it waits for another processor to release the resource, preventing wasting cycles repeating its request.

31. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emer as applied to claims 13-14 above, and further in view of Panwar.

32. As for Claim 15, Emer teaches all of the limitations inherited from Claim 13, but he does not teach that putting a processor to sleep comprises relinquishing of resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention

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to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

33. As for Claim 20, Emer teaches all of the limitations inherited from Claim 18, but he does not teach that putting a processor to sleep comprises relinquishing of resources. However, Panwar teaches that a sleeping virtual processor must release its resources to allow them to be used by other virtual processors (Column 8, Lines 33-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor of Emer release its resources as taught by Panwar in order to prevent itself from interfering with the execution of instructions for the other virtual processors (Panwar: Column 8, Lines 41-44).

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent Application Publication No. 2003/0163642.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571) 272-3634. The examiner can normally be reached on Monday - Thursday, 7:00-4:30; Alternate Fridays.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



JSC



**PAUL R. MYERS
PRIMARY EXAMINER**